REMARKS

Claims 1-6, and 8-25 are currently pending in this application. Claims 1-6, and 8-25 have been amended. Support for the Amendment may be found throughout the original claims and specification. It is believed that no new matter has been entered. Claim 7 is presently canceled without admission or prejudice.

Objection

Claim 23 was objected to for minor claim informalities. Claim 23 has been amended, and Applicants respectfully submit that the objection have been overcome.

Rejections Under 35 USC § 102

Claims 1-10, 12-19, and 24-25 are rejected under 35 USC 102(b) as being anticipated by Baddiley (US 4,852,065). However, as will set forth in detail below, it is submitted that none of the above cited claims are anticipated by Baddiley. Accordingly, these rejections are traversed and reconsideration is respectfully requested.

To anticipate, every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim. *Karsten Mfg. Corp. v. Cleveland Golf Co.* , 242 F3d 1376, 1383, 58 U.S.P.Q.2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 927 F.2d 1565, 1576, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). Further, the reference must describe the Applicant's claimed invention sufficiently to place a person of ordinary skill in the field of the invention in possession of it. *Akzo N.V. v. United States Int'l Trade Comm'n* , 808 F.2d 1471, 1479, 1 U.S.P.Q.2d 1241, 1245 (Fed. Cir. 1986), *cert denied*, 482 U.S. 909 (1987); *In re Coker*, 463 F.2d 1344, 1348, 175 U.S.P.Q. 26, 29 (CCPA 1972).

Baddiley fails to disclose, *inter alia*, a plurality of groups of memory cells within a matrix, wherein each group relates to a different size of data item. Baddiley also fails to disclose an enabling means having dedicated strobe connections to each of the plurality of groups of memory cells, wherein the enabling means is arranged to enable selected ones of the plurality of groups of memory cells, as determined by the size of the data items being transferred, to read data present at their inputs or to write stored data to their outputs in a single transfer operation.

Baddiley teaches a hardware configuration that is capable of handling only a fixed size of data item (e.g., 32 bit words only) (col. 1, line 64 to col. 2, line 21), and thus fails to teach a system that is capable of handling data items of variable size as presently claimed. Thus, because Baddiley fails to teach data items of variable size, it necessarily to fails to teach or suggest a grouping of memory cells according to the size of the data items. Furthermore, Baddiley also fails to disclose an enabling means having dedicated strobe connections to each of the plurality of groups of memory cells.

As Baddiley fails to disclose all of the limitations present in claim 1, Applicants assert that there is no anticipation of claim 1. Furthermore, because claims 2-9, 12-19, and 24-25 depend from claim 1, Applicants respectfully request that the rejection to all of these claims be withdrawn.

Rejections Under 35 USC § 103

Claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Baddiley in view of Kim et al. (US 6,781,898), hereinafter "Kim." Claims 20-23 was rejected under 35 U.S.C. 103(a) as being unpatentable over Baddiley in view of Glover (US 5,581,773). In light of the remarks below, these rejections are traversed and reconsideration is respectfully requested.

In order to establish a prima facie case of obviousness under §103, the Examiner has the burden of showing, by reasoning or evidence, that: 1) there is some suggestion or motivation, either in the references themselves or in the knowledge available in the art, to modify that reference's teachings; 2) there is a reasonable expectation on the part of one of ordinary skill in the art that the modification or combination has a reasonable expectation of success; and 3) the prior art references *teach or suggest* ***all*** the claim ***limitations***. (MPEP §2145, emphasis added).

As mentioned above, Baddiley fails to teach or suggest a plurality of groups of memory cells within a matrix, wherein each group relates to a different size of data item. Baddiley also fails to teach or suggest an enabling means having dedicated strobe connections to each of the plurality of groups of memory cells, wherein the enabling means is arranged to enable selected ones of the plurality of groups of memory cells, as determined by the size of the data items being transferred, to read data present at their inputs or to write stored data to their outputs in a single transfer operation.

As realized by the present inventors, in the context of providing a corner turning function, the grouping according to the size of the data item provides an overall increase speed of data transfer without facing the associated wiring costs/constraints. This is achieved in part because the redundant memory cells in a corner turning function can be ignored (Specification, pg. 3, lines 24-25).

Baddiley is directed toward reducing the width of a buffer store and thus the number of memory components. Thus, Baddiely would not suggest or motivate one of ordinary skill to increase the speed of data transfer within the memory cells. In fact, Baddiley teaches that it is desireable to maintain a constant speed of data transfer (col. 1, line 64 - col. 2, line 21). For example, according to Baddiley, if the width of the buffer is reduced by a factor of 16, the speed of the buffer is increased by a factor of four to maintain the overall data transfer speed. Thus, although Baddiely teaches that certain variables affect the data transfer speed, it teaches balancing out the parameter ranges maintain the same data transfer speed, rather than with the objective of increasing data transfer speed. Therefore, Baddiley would not lead one of ordinary skill to increase the speed of data transfer speed, and thus would not instruct one of ordinary skill to group the data items according to the size of the data item.

Although Applicants submit that Baddiley would not suggest or motivate one of ordinary skill to increase the data transfer speed, for the sake of argument, even if there were a motivation to do so, one of ordinary skill would likely increase the clock speed of the of the data transfer, rather than grouping the data items by the size. The increase in clock speed would allow increased data transfer speed without the wiring problems associated with the instantly claimed grouping.

The claimed grouping and the ability of the groupings to be individually activated enables higher data transfer speeds for different size data items. In other words, the present invention provides an efficient solution to increase the speed of a corner-turning data transfer function. Whilst, in the claimed invention, there is a theoretical possibility of wiring all possible memory cells to be selectively enabled and then selectively activating those required for efficient data transfer, there are wiring difficulties associated with this proposal. The wiring problem, and the additional advantage of the claimed solution is described in the instant specification on pg. 3,

line 21 - pg. 4, line 12. Neither the advantage of increasing the data transfer, nor the way which it can be realised is described in Baddiley. Thus, Applicants submit that Baddiley fails to teach or suggest a plurality of groups of memory cells within a matrix, wherein each group relates to a different size of data item. Baddiley also fails to teach or suggest an enabling means having dedicated strobe connections to each of the plurality of groups of memory cells, wherein the enabling means is arranged to enable selected ones of the plurality of groups of memory cells, as determined by the size of the data items being transferred, to read data present at their inputs or to write stored data to their outputs in a single transfer operation.

Kim is narrowly cited for teaching storing information in a matrix, wherein a shifting word pointer register is arranged to be controlled to skip the faulty row in the matrix and instead point to otherwise redundant additional row of the matrix. Glover is narrowly cited for teaching a masking register and an array of SIMD processors. None of the above cited refences rectify the above mentioned deficiences of Baddiley. Specifically, none of the above references teach or suggest a plurality of groups of memory cells within a matrix, wherein each group relates to a different size of data item.

Furthermore, Applicants submit that the presently claimed invention also provides advantages over the masking system disclosed in Glover. Previously, the best way to handle different data size items was to use variable position and size masks to provide data transfer into the memory as has been described in the introduction of the instant specification (pg. 2, lines 19-25). The improvement was to make the use of masking techniques redundant by configuring the memory into groups which relate to the different possible sizes of the data items which can be transferred. In this way, a two-step process of masking, and then transferring, can be replaced with a single transfer step into the selectively enabled group of memory locations. Glover fails to teach or suggest an enabling means arranged to enable selected ones of the plurality of groups of memory cells to read data present at their inputs or to write stored data to their outputs in a single transfer operation.

Accordingly, none of the cited references, either alone or combination, teach or suggest all of the elements of claims 11, and 20-23 as required by 103(a). Thus, withdrawal of the rejection of claims 11, and 20-23 under 35 U.S.C. 103(a) is thus respectfully requested.

CONCLUSION

Applicant respectfully submits that the currently pending claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
DINSMORE & SHOHL LLP

By /Jacob P. Woolbright/
Jacob P. Woolbright
Registration No. 64,426

Fifth Third Center
One South Main Street, Suite 1300
Dayton, Ohio 45402-2023
Telephone: (937) 449-6400
Facsimile: (937) 449-6405

JPW/AMM/tlo